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10EC63

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast THREE questions from Part-A and any TWO questions from Part-B.***

PART – A

1 a. Derive the expression for i_D in saturation and triode region with the neat diagram. Explain the effect of increase in drain to source voltage after saturation. **(10 Marks)**

b. Why large signal model is required? Explain the large signal model of NMOS. **(04 Marks)**

c. Determine the value of R_D, which is required for maintaining saturation region for the following circuit. The transistor operates in saturation with $I_D = 0.5mA$ and $V_D = +3V$. Let the enhancement type PMOS transistor have $v_t = -1V$ and $K'_n(W/L) = 1mA/m^2$ and assume $\lambda = 0$. **(06 Marks)**

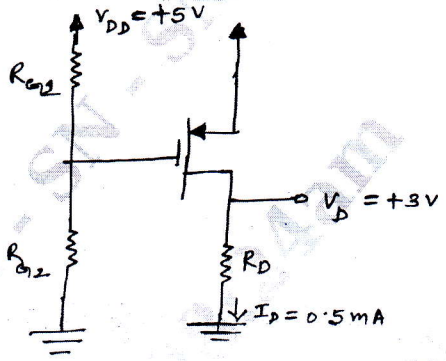

Fig.Q.1(c)

2 a. Explain the effect of denegative resistance in biasing by fixing V_G and connecting resistance in the source. Compare the other biasing. **(10 Marks)**

b. What is source follower? Derive the voltage gain and overall voltage equations of a source follower using MOSFET. **(10 Marks)**

3 a. Mention any 4 comparison of important characteristics of MOSFET and the BJT. **(04 Marks)**

b. Explain different types of short channel in scaling MOSFET. **(06 Marks)**

c. Draw the MOSFET constant current source circuit and explain it along with advantage. **(10 Marks)**

4 a. Explain the operation of a MOS cascade amplifier. Mention its advantage and obtain an expression for short circuit trans conductance GM. **(10 Marks)**

b. Derive the voltage gain expression for CMOS implementation of CS amplifier. **(10 Marks)**

5 a. Show that CMRR of perfectly matched MOS differential amplifier with a common mode input signal V_{icm} is infinite. **(10 Marks)**

b. Explain the basic MOS differential pair operation. **(10 Marks)**

PART – B

6 a. Explain four basic feedback topologies with neat diagram. (08 Marks)
b. Explain briefly with expression the properties of negative feedback. (08 Marks)
c. Draw general structure of feedback amplifier. (04 Marks)

7 a. Why non inverting configuration of Op-amp is called as voltage follower amplifier. Explain the operation with equivalent circuit model. (06 Marks)
b. Show that CMRR of a single Op-amp difference amplifier is finite. (10 Marks)
c. Discuss the effect of finite open-loop gain of an inverting configuration of Op-amp. (04 Marks)

8 a. Explain the parameters required to characterize the operation and performance of logic circuit family. (10 Marks)
b. Implement $F = \overline{AB + CD}$ using the AOI Gate. (06 Marks)
c. Write the circuit for a two-input CMOS NOR gate and a two-input CMOS NAND gate. (04 Marks)

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